TPS54680EVM-228 6-Amp, TPS54880EVM-228 8-Amp, SWIFT ™ Regulator Evaluation Module

User's Guide

November 2002

PMP EVMs

SLVU077

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User’s Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the TPS54x80EVM-228 SWIFT™ regulator evaluation module (EVM) and contains the EVM schematic, bill of materials, assembly drawing, and board layouts.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials
- Appendix A—Out of Phase Synchronization of I/O and Core SWIFT™ Famly Regulators

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Contents

1 Introduction 1-1
- 1.1 Background 1-2
- 1.2 Performance Specification Summary 1-4
- 1.3 Tracking Regulator and Power Sequencing 1-6
- 1.4 Modifications 1-7
  - 1.4.1 Output Voltage 1-7
  - 1.4.2 Switching Frequency 1-7

2 Test Setup and Results 2-1
- 2.1 Input/Output Connections 2-2
- 2.2 Power Sequencing Test 2-4
- 2.3 Efficiency 2-8
- 2.4 Power Dissipation 2-9
- 2.5 Output Voltage Regulations 2-10
- 2.6 Load Transients 2-11
- 2.7 Loop Characteristics 2-12
- 2.8 Output and Input Voltage Ripple and Main Switching Waveforms 2-13

3 Board Layout 3-1
- 3.1 Layout 3-2

4 Schematic and Bill of Materials 4-1
- 4.1 Schematic 4-2
- 4.2 Bill of Materials 4-3

A Out of Phase Synchronization of I/O and Core SWIFT Family Regulators A-1

Figures

1-1 Different Power Sequencing Technique Selection 1-6
1-2 Frequency Trimming Resistor Selection Graph 1-8
2-1 Connection Diagram 2-3
2-2 Powering Up With Tracking 2-4
2-3 Powering Down With Tracking 2-5
2-4 Powering Up With Ratiometric Sequencing 2-6
2-5 Powering Down With Ratiometric Sequencing 2-6
2-6 Powering Up With Core Voltage Rising FIrst 2-7
2-7 Powering Down With Core Voltage Falling Second 2-7
2-8 Measured Efficiency 2-8
2-9 Measured Board Losses 2-9
2-10 Load Regulation 2-10
2-11 Line Regulation 2-10
2-12 Load Transient Response at Input Voltage 3.3 V, TPS54680 2-11
2-13 Load Transient Response at Input Voltage 5 V, TPS54680/TPS54880 2-11
2-14 Measured Loop Response, TPS54680, V_I = 3.3 V, V_O = 1.8 V 2-12
2-15 Measured Loop Response, TPS54680 and TPS54880, V_I = 5 V, V_O = 1.8 V 2-12
2-16 Input and Output Voltage Ripple and Main Switching Waveform at V_I = 3.3 V 2-13
2-17 Input and Output Voltage Ripple and Main Switching Waveform at V_I = 5 V 2-14
3-1 Top Side Assembly 3-2
3-2 Top SIde Layout 3-3
3-3 Internal Layer 2 Layout 3-3
3-4 Internal Layer 3 Layout 3-4
3-5 Bottom Side Layout (looking from top side) 3-4
4-1 TPS54x80EVM-228 Schematic 4-2
A-1 Input Voltage Ripple and Main Switching Waveforms at V_I = 5 V of Two Regulators Switching at 15% Apart Frequencies A-1
A-2 Input Voltage Ripple (Ch2),Sync Signal (Ch3) and Switching Waveforms of Core Regulator (Ch4) and I/O Regulator (Ch1) A-2
A-3 Input Voltage Ripple (Ch2)and Switching Waveforms of Synchronized Out of Phase Core Regulator (Ch4) and I/O Regulator (Ch1) A-3
A-4 Input Voltage Ripple (Ch2 and Switching Waveforms of Nonsynchronized Core Regulator (Ch4) and I/O Regulator (Ch1) A-3

Tables

1-1 Input Voltage and Output Current Summary 1-3
1-2 TPS54680EVM-228 Performance Specification Summary 1-4
1-3 TPS54880EVM-228 Performance Specification Summary 1-5
1-4 Output Voltage Programming 1-7
4-1 TPS54x80EVM-228 Bill of Materials 4-3

Chapter 1

Introduction

This chapter contains background information for the TPS54680 and TPS54880 as well as performance specifications and support documentation for the TPS54680EVM-228, TPS54880EVM-228 evaluation modules (SLVP228). Different types of power sequencing and implementation using TPS54x80 tracking regulators are described.

Topic **Page**

1.1 Background 1-2

1.2 Performance Specification Summary 1-4

1.3 Tracking Regulator and Power Sequencing 1-6

1.4 Modifications 1-7

1.1 Background

The SWIFT™ family TPS54680 and TPS54880 tracking dc/dc converters are designed to provide accurate power sequencing in applications where two or more voltages are required for a load. These types of applications include core and I/O power supplies for microprosessors, DSPs and FPGAs. Typically, some specific relation between the core and I/O supply voltages has to be provided during the power-up and power-down sequences. The TPS54x80 family of tracking dc/dc converters is capable of direct tracking, ratiometric tracking, and voltage sequencing with a second power source. The TPS54680EVM-228 evaluation module uses a TPS54680 tracking dc/dc converter paired with a TPS54610 dc/dc converter to provide a two output supply at 6 A per channel, while the TPS54880EVM-228 pairs a TPS54880 with a TPS54810 providing 8 A per channel. The TPS54x80EVM-228 provides a 3.3-V output voltage for I/O, and 1.8 V for the core at a nominal 5-V input. The TPS54x10 dc/dc converters are used in this EVM as an example only. Any other switching or linear regulator can be used for this application. These two-channel EVMs demonstrate the flexibility inherent in the TPS54x80 design for tracking and sequencing core and I/O voltages.

The TPS54680 and TPS54880 devices use the TRACKIN pin to access the tracking and sequencing capabilities. An internal multiplexer circuit compares the voltage at this pin with the internal reference voltage and uses the lesser of the two as the reference for the output voltage regulation. When the output of another power supply or distribution switch is connected to the TRACKIN pin of TPS54x80, the output of the TPS54x80 tracks the output of this other channel during power up or down, until the voltage at TRACKIN pin becomes higher then the internal reference voltage. By applying the other power supply output to the TRACKIN pin through an appropriate resistor divider network, any required power-up and power-down relation between two output voltages of regulators can be set by changing the ratio of the divider network.

In some applications the 3.3-V bus for the I/O supply voltage is available and there is no need for an additional voltage regulator. In this case, the 3.3-V bus can be used as the input voltage for the tracking regulator TPS54x80. The I/O voltage may be supplied through a distribution switch providing reasonable rise times and preventing large inrush currents. The TRACKIN pin of TPS54x80 must be connected to the output of the distribution switch to provide proper power sequencing.

Both channels of this TPS54x80EVM-228 evaluation module can be synchronized out of phase by using a small number of inexpensive external components. Synchronization is useful both to decrease unwanted beat frequencies and reduce the ripple current in the input capacitors. The synchronization is especially effective if the load current of both channels do not differ significantly from each other. The synchronization circuit is optional and it may not be needed in many applications, however the circuit is provided on the evaluation module. The rated input voltage and output current range for this EVM is given in Table 1-1.

These evaluation modules are designed to demonstrate the small PCB area that may be achieved when designing with the SWIFT™ family of regulators.

The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.65 µH output inductor. The MOSFETs of the SWIFT™ regulators are incorporated inside the package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the SWIFT™ regulators high efficiency and helps to keep the junction temperature low at high output currents. It is important to note that the SWIFT™ integrated FET dc/dc converters provide true thermal protection of the whole circuit. Controllers utilizing external FETs thermally protect only the controller itself, not the FETs. The compensation components of TPS54x80 regulators are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54680EVM-228	4.3 V to 6 V†	0 A to 6 A
TPS54880EVM-228	4.5 V to 6 V	0 A to 8 A

† The minimum input voltage in this EVM is limited by the 3.3 V output of regulator TPS54X10. The input voltage should be always above the output voltage plus an additional margin because of voltage drops in power stage and limited maximum duty cycle. The data sheet specifies the minimum input voltage of TPS54680 regulator as 3 V. The minimum input voltage of TPS54880 regulator is 4 V.

1.2 Performance Specification Summary

A summary of the TPS54x80EVM-228 performance specifications is provided in Table 1-2 and Table 1-3. These data relate only to core voltage outputs of the TPS54680 and TPS54880. The performance specification summaries for the TPS54610 and TPS54810 can be found in the related User's Guide, TI literature number SLVU071. All specifications are given for an ambient temperature of 25°C, unless otherwise noted

Table 1-2. TPS54680EVM-228 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4.3[†]	5.0	6.0	V
Output voltage set point range		0.9	1.8	3.3	V
Output current range		0		6	A
Line regulation	I_O = 0 A and 6 A	-0.2%		0.2%	
Load regulation	V_{IN} = 5 V	-0.2%		0.2%	
Load transient response	I_O = 1.5 A to 4.5 A, t(rise) = 1 µs, V_{IN} = 5 V		-60		mV_{PK}
			20		µs
	I_O = 4.5 A to 1.5 A, t(fall) = 1 µs, V_{IN} = 5 V		80		mV_{PK}
			20		µs
Loop bandwidth	V_{IN} = 5 V		100		kHz
Phase margin	V_{IN} = 5 V		50		°
Input ripple voltage with synchronized channels	V_{IN} = 5 V, I_O = 6 A		110		mV_{PP}
Input ripple voltage with nonsynchronized channels	V_{IN} = 5 V, I_O = 6 A		160		mV_{PP}
Output ripple voltage			10		mV_{PP}
Tracking delay			10		µs
Operating frequency			700		kHz
Maximum efficiency	V_{IN} = 5.0 V, I_O = 2.5 A, Vout = 1.8 V		89%		
Efficiency at I_O = 6 A	V_{IN} = 5.0 V, Vout = 1.8 V		85%		

† The minimum input voltage in this EVM is limited by the 3.3 V output of regulator TPS54610. The minimum input voltage of regulators TPS54680 and TPS54610 is 3 V.

Table 1-3. TPS54880EVM-228 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4.5†	5.0	6.0	V
Output voltage set point range		0.9	1.8	3.3	V
Output current range		0		8	A
Line regulation	I_O = 0 A-8 A	-0.2%		0.2%	
Load regulation	V_{IN} = 5 V	-0.2%		0.2%	
Load transient response	I_O = 1.5 A to 4.5 A, t(rise) = 1 µs, V_{IN} = 5 V		-60		mV_{PK}
			20		µs
	I_O = 4.5 A to 1.5 A, t(fall) = 1 µs, V_{IN} = 5 V		80		mV_{PK}
			20		µs
Loop bandwidth	V_{IN} = 5 V		100		kHz
Phase margin	V_{IN} = 5 V		50		°
Input ripple voltage with synchronized channels	V_{IN} = 5 V, I_O = 8 A		110		mV_{PP}
Input ripple voltage with nonsynchronized channels	V_{IN} = 5 V, I_O = 8 A		160		mV_{PP}
Output ripple voltage			10		mV_{PP}
Tracking delay			10		µs
Operating frequency			700		kHz
Maximum efficiency	V_{IN} = 5.0 V, I_O = 2.5 A, Vout = 1.8 V		89%		
Efficiency at I_O = 8 A	V_{IN} = 5.0 V, Vout = 1.8 V		82%		

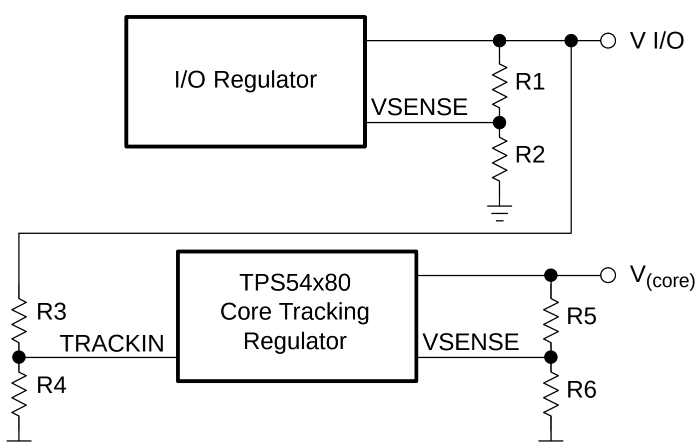
† The minimum input voltage in this EVM is limited by the 3.3-V output of regulator TPS54810. The minimum input voltage of regulators TPS54880 and TPS54810 is 4 V.

1.3 Tracking Regulator and Power Sequencing

To avoid potential problems with the processor and system ICs, designers can apply three general techniques for power-up sequencing: sequential, ratiometric, or simultaneous. Sequential power up, as the name implies, powers up the two rails one after the other. Typically the second rail begins to ramp up once the first rail reaches regulation. Alternately, the second rail may begin its ramp after a set delay from the start of the first rail. Either method must comply with the processor manufacturer's restriction on the minimum and maximum time one supply is not powered, or the duration and amount that one supply exceeds the other. With the second or ratiometric method, the two rails begin to power up and reach regulation at the same time. This requires a higher slew rate for the rail with the higher final voltage, and results in the maximum voltage differential occurring when regulation is reached. However, some processors may not tolerate the instantaneous voltage differences that occur before regulation is reached, or the processor may draw high current from one supply during this period. The third approach eliminates instantaneous voltage differences and minimizes the magnitude and duration of stresses. A common way of implementing this method is simultaneous power up, in which the voltage rails rise together and at the same rate, with the higher or I/O voltage rail continuing after the lower or core voltage rail has reached its final value.

The TPS54x80EVM-228 evaluation module is designed to demonstrate the described power sequencing technique. The basic idea is shown in Figure 1-1.

Figure 1-1. Different Power Sequencing Technique Selection



Implementation of different power sequencing techniques is based on proper resistor-divider ratio selection. The equations 1, 2, and 3 provide related ratios for different ways of power sequencing.

$$\frac{R3}{R4} = \frac{R5}{R6} \quad \text{– core voltage tracks I/O voltage (simultaneous power up)} \tag{1}$$

$$\frac{R3}{R4} = \frac{R1}{R2} \quad \text{– ratiometric relation between core and I/O voltage} \tag{2}$$

$$\frac{R3}{R4} < \frac{R5}{R6} \quad \text{– core voltage rises first at power up and falls second at power down.} \tag{3}$$

1.4 Modifications

The TPS54x80EVM-228 evaluation module is designed to demonstrate the small size using ceramic capacitors that can be attained when designing with the TPS54x80. Meanwhile, the solution is not limited only to these particular output voltages and switching frequency. The following paragraphs describe what kind of modifications can be done to meet different application requirements.

1.4.1 Output Voltage

The 1.8-V core and 3.3-V I/O output voltage is selected for this EVM. The output voltage of the TPS54x80 and TPS54X10 regulators can be adjusted to any value down to 0.9 V by changing resistor R20 (for the TPS54x80) or R19 (for the TPS54x10). The location of these resistors in the schematic is shown in Figure 4-1. The value of these resistors for a specific output voltage can be calculated by using equation 4. Table 1-4 lists the value of resistor R19 (or R20) for some common bus voltages.

$$R_{19,\,20} = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \tag{4}$$

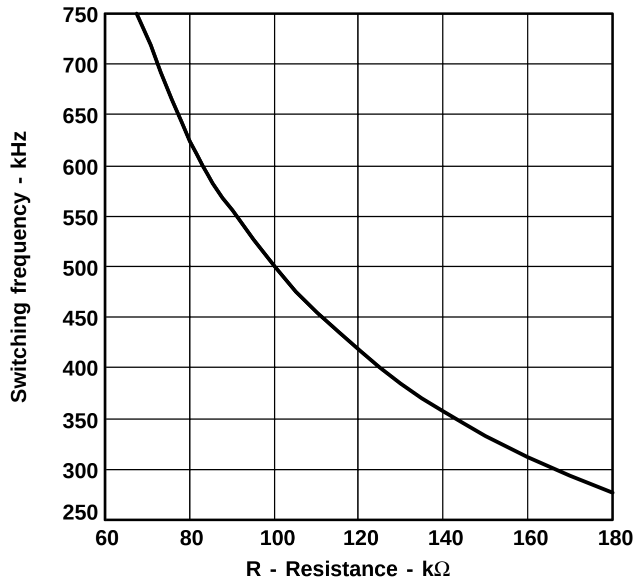
Table 1-4. Output Voltage Programming

Output Voltage, (V)	R19 or R20, (kΩ)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

1.4.2 Switching Frequency

The switching frequency of TPS54x80 and TPS54x10 regulators may be trimmed to any value between 280 kHz and 700 kHz by changing the value of resistors R9 (for TPS54x80) or R8 (for TPS54x10). The location of these resistors in the schematic is shown in Figure 4-1. Increasing the switching frequency reduces the output ripple. It is not recommended to decrease the switching frequency for the selected output filter in this EVM below 600 kHz. The nominal switching frequencies in SLVP228 EVM are set about 20% apart for each channel to synchronize the I/O regulator to the higher switching frequency of the core regulator. If there is no need to synchronize channels, and synchronization circuit parts are left open, then it is recommended to use 71.5 kΩ value resistor for R8, the same value as R9. A plot of the value of resistors R8 (or R9) versus the switching frequency is given in Figure 1-2.

Figure 1-2. Frequency Trimming Resistor Selection Graph



Chapter 2

Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54x80EVM-228 evaluation module. The chapter also includes test results typical for the TPS54x80EVM-228 and covers efficiency, overall power dissipation, output voltage regulation, load transients, loop response, output ripple, input ripple, and different ways of power sequencing and tracking during power up and power down.

Topic **Page**

2.1	**Input/Output Connections**	**2-2**
2.2	**Power Sequencing Test**	**2-4**
2.3	**Efficiency**	**2-8**
2.4	**Power Dissipation**	**2-9**
2.5	**Output Voltage Regulations**	**2-10**
2.6	**Load Transients**	**2-11**
2.7	**Loop Characterisitcs**	**2-12**
2.8	**Output and Input Voltage Ripple and Main Switching Waveforms**	**2-13**

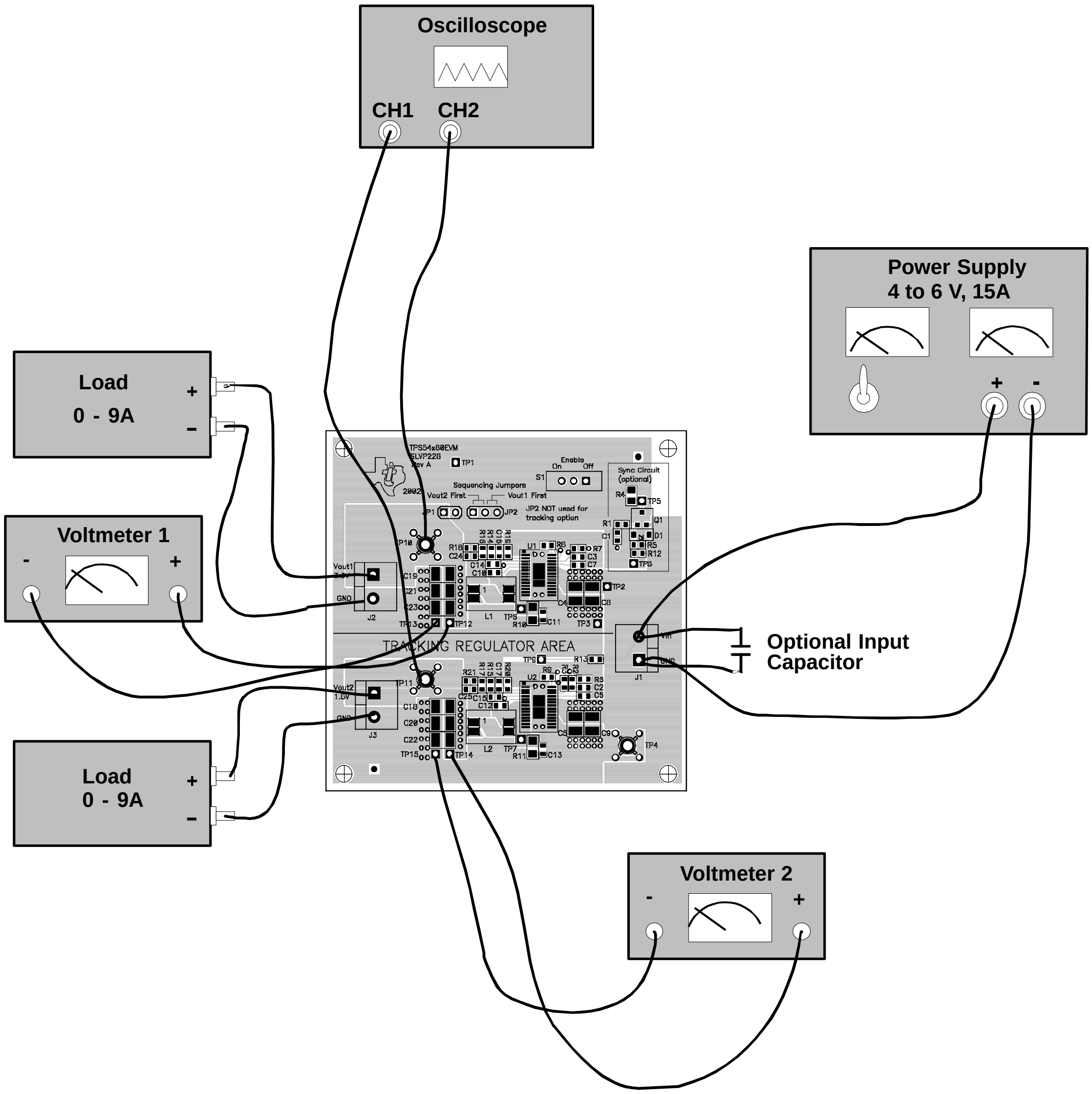
2.1 Input/Output Connections

The TPS54x80EVM-228 has the following input/output connections: 5-V input, 5-V input return, 3.3-V output, 3.3-V output return, 1.8-V output and 1.8-V output return. A diagram showing the connection points is shown in Figure 2-1. A power supply capable of supplying 15 A should be connected to J1 through a pair of 16 AWG wires. The 3.3-V and 1.8-V loads should be connected respectively to J2 and J3 through pairs of 16 AWG wires. The maximum load current may be reduced from 8 A to 6 A, if the 6-A version of the TPS54x80EVM-228 with TPS54680/TPS54610 regulators is used. Wire lengths should be minimized to reduce losses in the wires. Test points TP10 and TP11 provide a place to easily connect an oscilloscope voltage probe to monitor the output voltages, while TP4 provides a test point for monitoring the input voltage. The TPS54x80 device is intended to be used as a point of load regulator typically located close to the input voltage source. When using the TPS54x80EVM-228 with an external laboratory power supply as the source for Vin, an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hookup wires. The presented test results were obtained using a 470 µF, 16 V additional input capacitor.

IMPORTANT NOTICE:

The two-channel TPS54x80EVM-228 EVM requires an input voltage of 4.5-V to 6-V to provide 3.3-V output from the TPS54610/TPS54810 regulators for I/O voltage. Stand-alone measurements of TPS54680 regulator operating at a 3.3-V input voltage are also provided for reference. The TPS54680 has a rated input voltage range of 3.0 to 6.0 V, and may be powered from a 3.3-V bus in some applications.

Figure 2-1. Connection Diagram

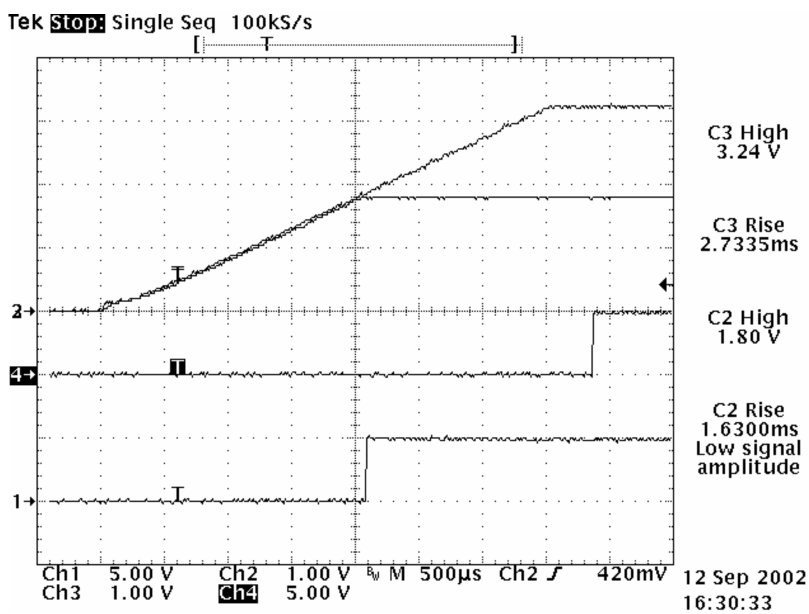


2.2 Power Sequencing Test

The TPS54x80 regulators provide different modes for power-up and power-down sequencing of the core and I/O voltages. By selecting the different ratios for the resistor divider R3/R6 (Figure 4-1), the slope of the core voltage during power up and down can be set equal to, higher than, or lower than the slope of I/O voltage. If the resistors R6 = R20 and R3 = R21, then the core voltage tracks the I/O voltage. The start-up voltage waveform of the TPS54x80EVM-228 for this condition is shown in Figure 2-2. The waveform shows that the core voltage regulator tracks the output of the I/O regulator until the core regulator reaches its nominal 1.8-V level. After that, the core regulator starts to regulate its output at the preset 1.8-V level. The I/O regulator continues its ramp-up until the voltage reaches the nominal 3.3-V level. The output voltage waveforms during power up do not depend on load currents. These output voltage waveforms are the same for two different ways of powering up—by applying the input voltage with the ENABLE signals for both channels asserted, or by asserting the ENABLE signal while the input voltage is already applied. For these tests:

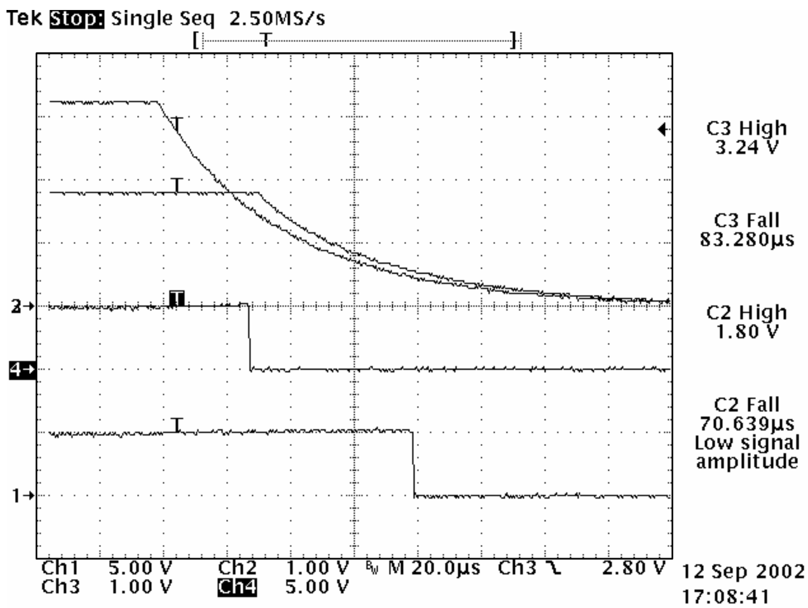
Ch.2: Output voltage of TPS54x80 (1.8 V) 1 V/div.
Ch.3: Output voltage of TPS54x10 (3.3 V) 1 V/div.
Ch.1: Power Good signal of TPS54x80 5 V/div.
Ch.4: Power Good signal of TPS54x10 5 V/div.
Time: 500 μs/div.

Figure 2-2. Powering Up With Tracking



The powering down waveform, by using the ENABLE signal, is shown in Figure 2-3. During power down, the fall time of output voltage depends on the output capacitance and load resistance. In this case a very low resistance (0.5 Ω) I/O output load has been selected to show the dynamic performance of the TPS54x80. It is seen that even if the I/O output voltage falls with the slew rate of about 75 V/ms, there is less than 0.3-V difference between the core voltage and I/O voltage. This difference and some delay are caused by the response time of the feedback loop of tracking regulator. For most applications the I/O voltage falls much slower and the difference between core and I/O voltage becomes negligible. Notice that power down by removing the input voltage may not provide proper power sequencing below undervoltage lockout limit where the both integrated switches are off. So, using the ENABLE signal for power down is the preferred option for power sequencing.

Figure 2-3. Powering Down With Tracking



The TPS54x80EVM-228 EVM provides the ability to change the slew rate of output voltage of the core regulator by using jumper JP2 (see schematic in Figure 4-1). If jumper JP2 is set so that R2 is connected in parallel to R6, ratiometric power sequencing is implemented. For ratiometric sequencing, the following condition needs to be met: R3 = R18 and R2 II R6 = R19. In this case the I/O and core voltages reach their nominal values at the same time. The waveforms for ratiometric powering up and down are shown in Figure 2-4 and Figure 2-5.

Figure 2-4. Powering Up With Ratiometric Sequencing

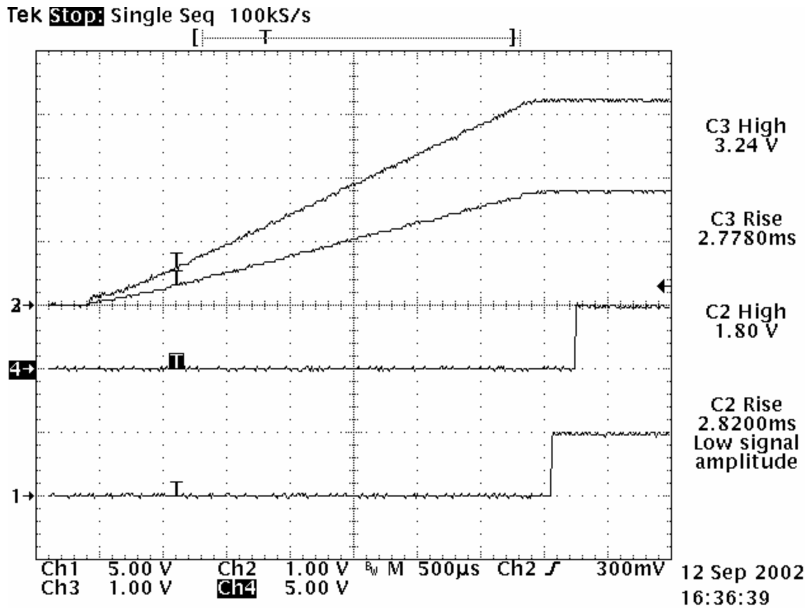
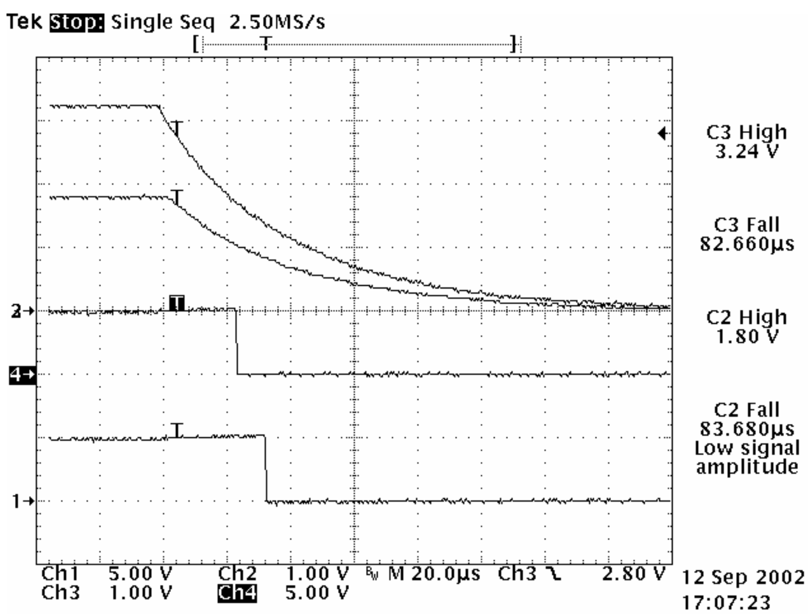


Figure 2-5. Powering Down With Ratiometric Sequencing



If jumper JP2 is set so that R2 is connected in parallel to R3, the core voltage rises first during power up, i.e. prior to the I/O voltage rise, and falls second during power down. The waveforms with this type of sequencing are shown in Figure 2-6 and Figure 2-7.

Figure 2-6. Powering Up With Core Voltage Rising FIrst

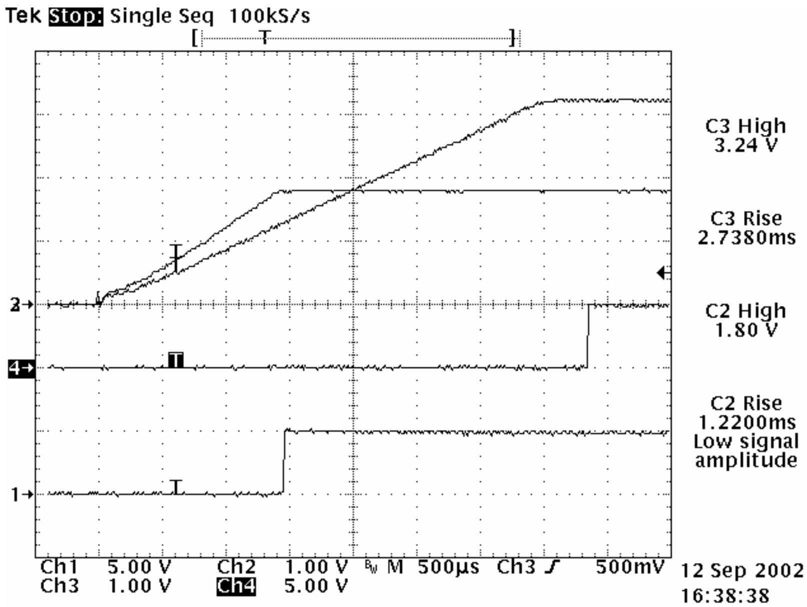
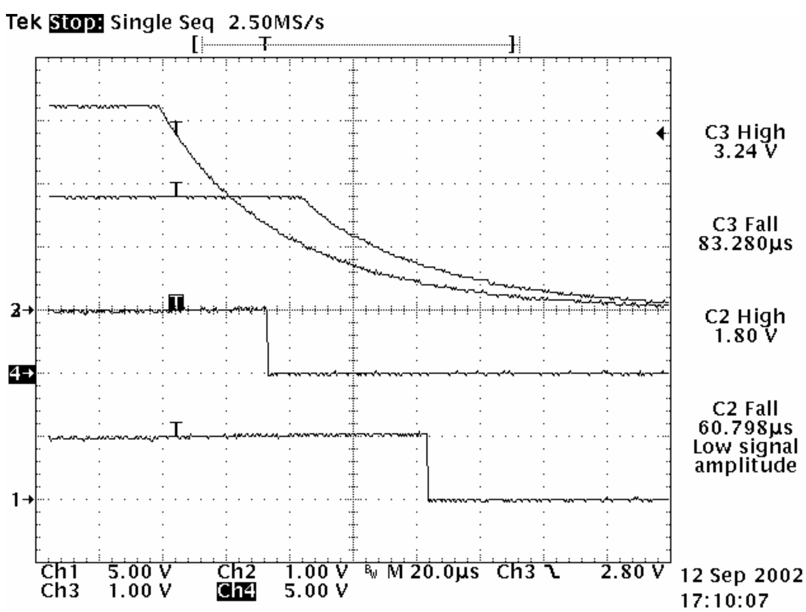


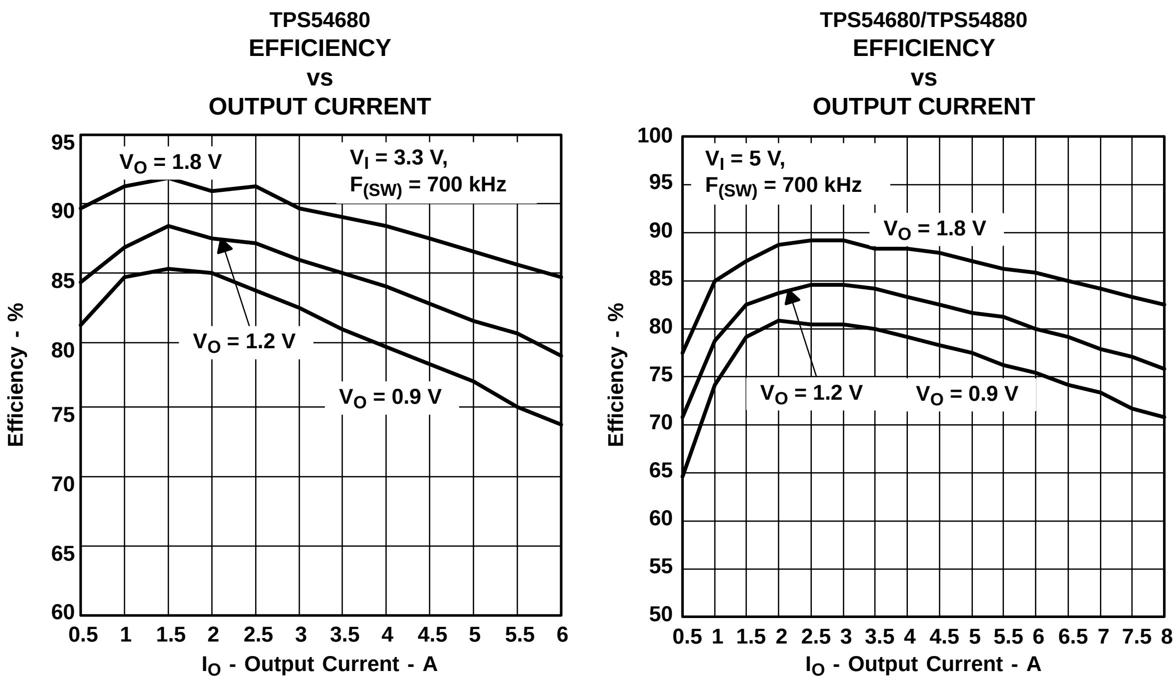
Figure 2-7. Powering Down With Core Voltage Falling Second



2.3 Efficiency

The TPS54x80EVM-228 efficiency depends on output voltage, even though the power losses are roughly the same for any output voltage. Efficiency also depends on input voltage. For the output current below 3 A, the efficiency is higher at 3.3-V input voltage because of lower switching losses. For the output current above 3 A, the efficiency is better at 5-V input voltage because of lower drain-to-source resistance of integrated FETs driven by higher gate voltage. The efficiency shown in Figure 2-8 is for 5-V input (TPS54680, TPS54880) and 3.3-V input (TPS54680) at ambient temperature of 25°C.

Figure 2-8. Measured Efficiency



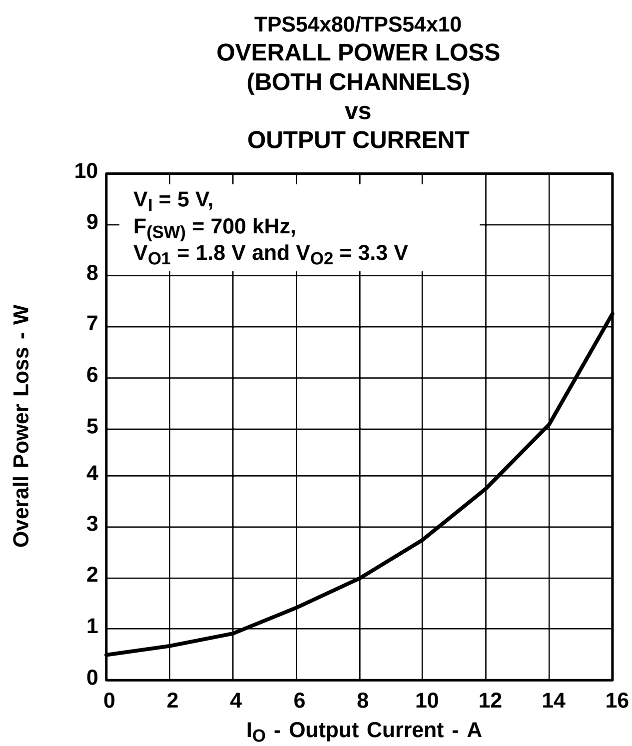
The input current, consumed by 3.3-V output regulator TPS54x10, is excluded from these data. The measurements relate only to the core voltage channel provided by tracking regulators TPS54680 and TPS54880. Efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies, due to the switching losses in the MOSFETs.

2.4 Power Dissipation

The low junction-to-case thermal resistance of the PWP package with PowerPad™, along with a good board layout, allows the TPS54x80EVM-228 to provide full rated load current while maintaining safe junction temperatures. The total board losses at 25°C are shown in Figure 2-9. The input voltage is 5 V. The load current shown in the Figure 2-3 is the sum of currents of both core and I/O regulators.

The temperature rise of PowerPad™, which is only few degrees below the junction temperature, has been measured at 6 A (TPS54680/TPS54610) and 8 A (TPS54880/TPS54810) loads. At 6-A load current from each channel, the temperature rise does not exceed 33°C and at 8 A the measured temperature rise was 54.2°C. The overall dissipated power for these two conditions is 3.8 W and 7.2 W respectively. These test data are taken without airflow at room temp 22°. For the additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2-9. Measured Board Losses



2.5 Output Voltage Regulations

The output voltage load regulation of the TPS54x80EVM-228 is shown in Figure 2-10, while the output voltage line regulation is shown in Figure 2-11. Measurements are given for an ambient temperature of 25°C.

Figure 2-10. Load Regulation

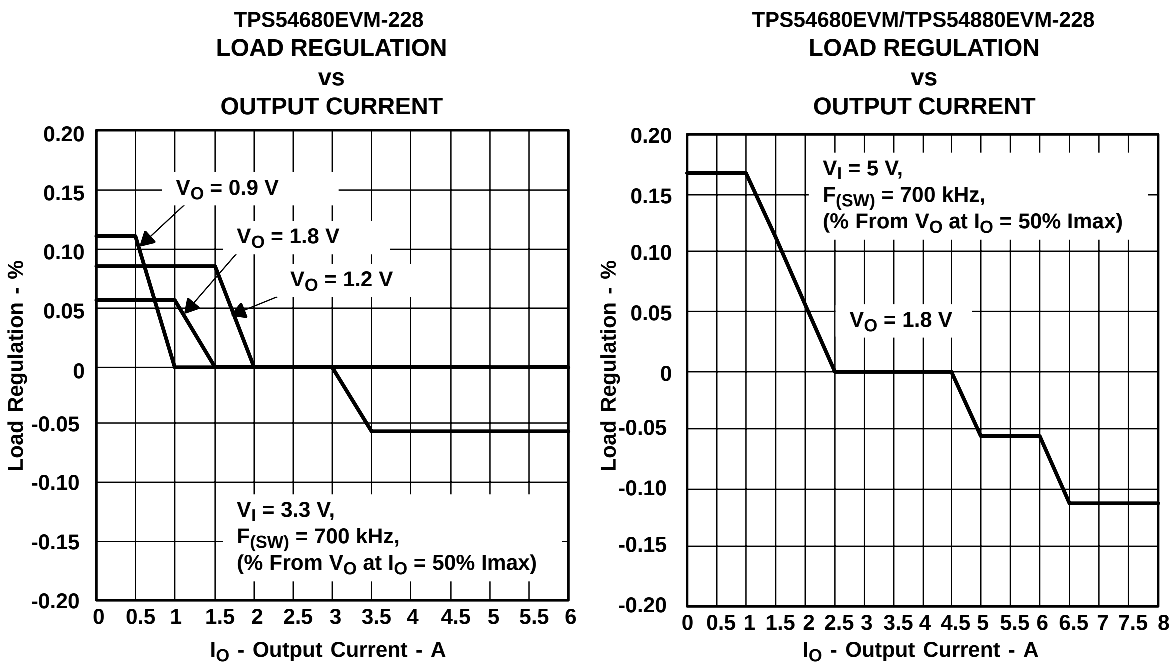
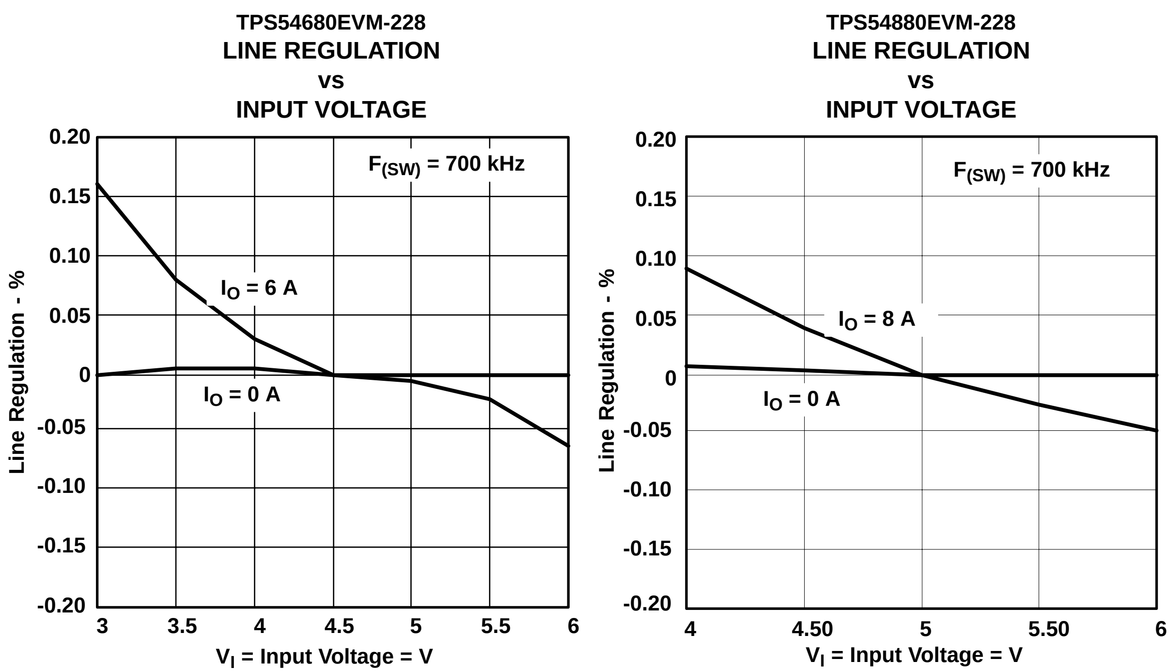


Figure 2-11. Line Regulation



2.6 Load Transients

TPS54x80EVM-228 response to load transients is shown in Figure 2-12 and Figure 2-13. The current step is from 1.5 A to 4.5 A with the slew rate 5A/µs. For these measurements:

Ch.2: Output voltage 100 mV/div.
Ch.4: Load current 2 A/div.
Time: 20 µs/div.

Figure 2-12. Load Transient Response at Input Voltage 3.3 V, TPS54680

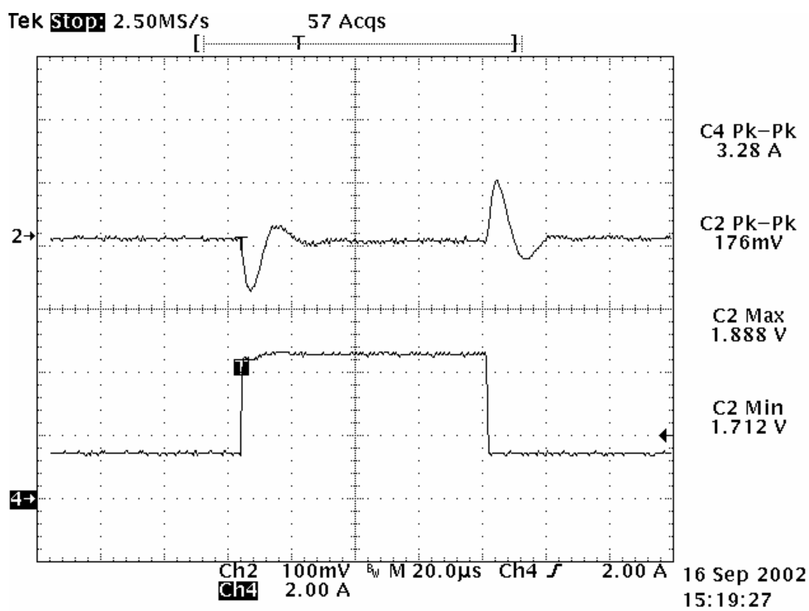
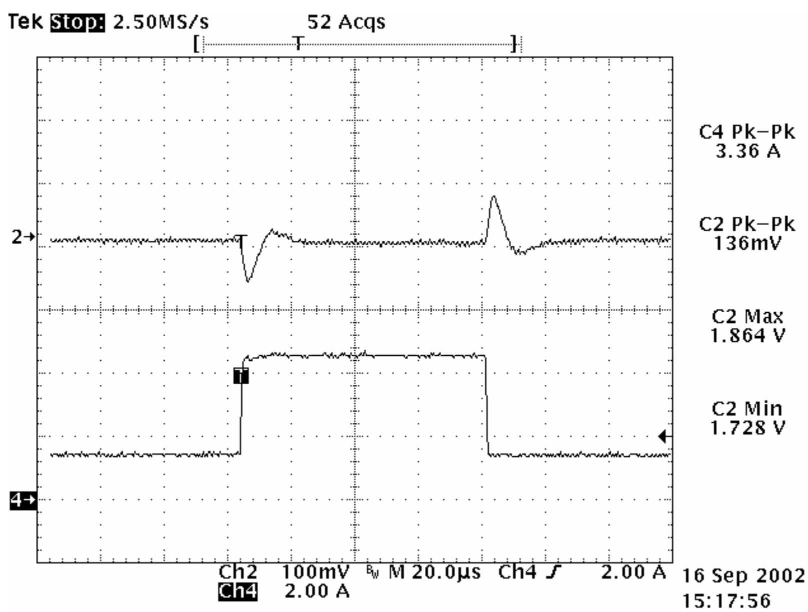


Figure 2-13. Load Transient Response at Input Voltage 5 V, TPS54680/TPS54880



2.7 Loop Characteristics

The TPS54x80EVM-228 loop response characteristics are shown in Figure 2-14 and Figure 2-15. Gain and phase plots are shown at 3.3 V for TPS54680 and at 5 V for TPS54680 and TPS54880 regulators.

Figure 2-14. Measured Loop Response, TPS54680, V_I = 3.3 V, V_O = 1.8 V

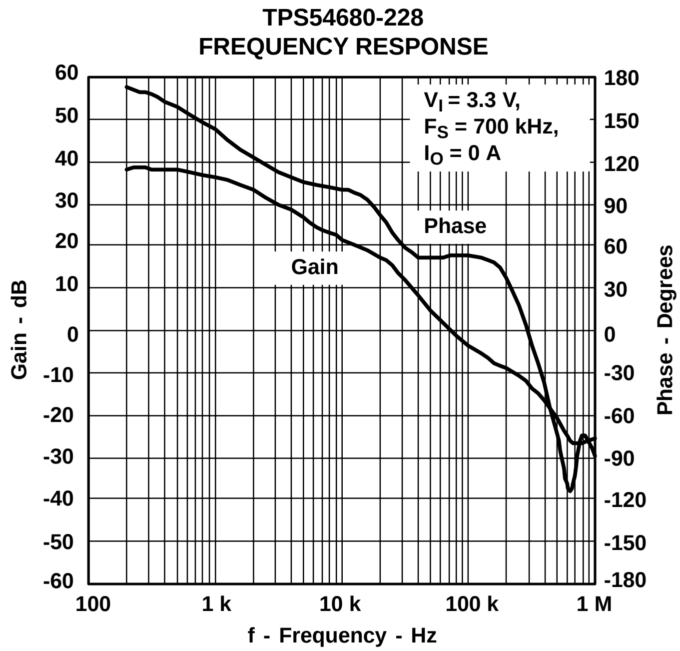
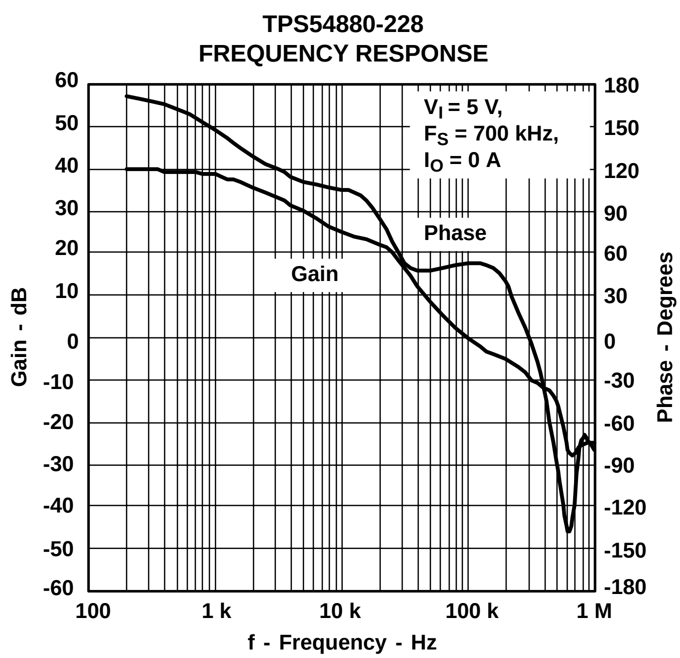


Figure 2-15. Measured Loop Response, TPS54680 and TPS54880, V_I = 5 V, V_O = 1.8 V



2.8 Output and Input Voltage Ripple and Main Switching Waveforms

The TPS54x80EVM-228 evaluation module output and input voltage ripple and main switching waveforms at V_I = 3.3 V, V_O = 1.8 V, I_O = 6 A and Fs = 700 kHz are shown in Figure 2-16. For these waveforms for the TPS54680 regulator:

Ch.2: Input ripple 100 mV/div.
Ch.3: Output ripple 20 mV/div.
Ch.4: Phase pin 2 V/div.
Time: 1 µs/div

Figure 2-16. Input and Output Voltage Ripple and Main Switching Waveform at V_I = 3.3 V

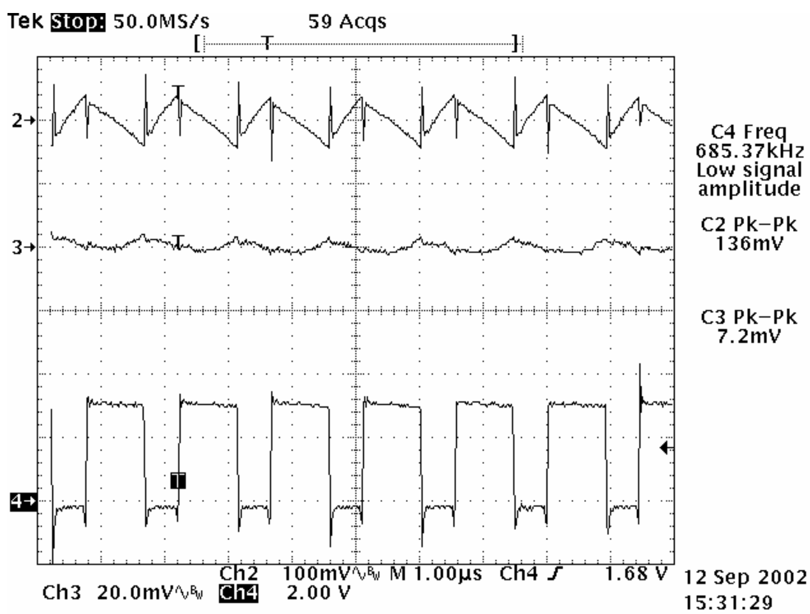
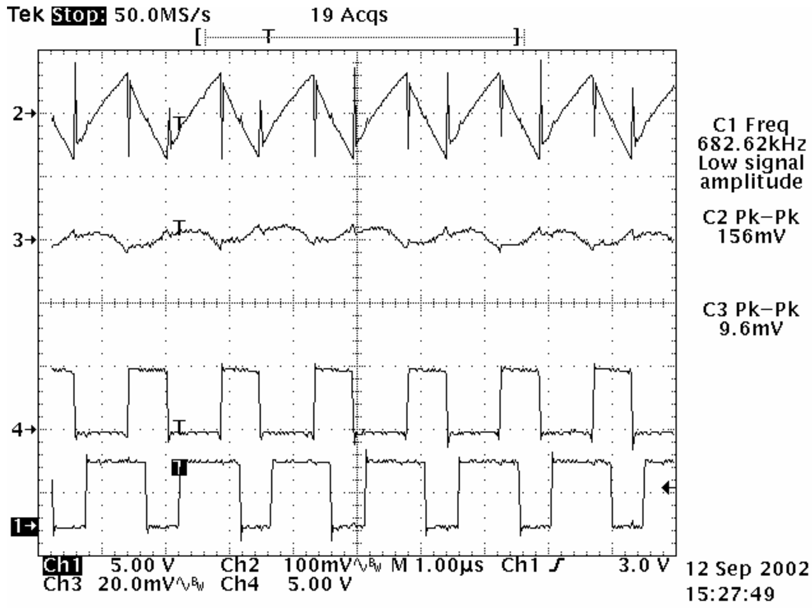


Figure 2-17 shows the output and input voltage ripple and main switching waveforms of the core regulator TPS54680/TPS54880 and I/O regulator TPS54610/TPS54810. The measurements are taken at V_I = 5 V, V_O = 1.8 V (core), I_O = 6 A (core), V_O = 3.3 V (I/O), I_O = 0 A (I/O) and Fs = 700 kHz for both channels. For these waveforms:

Ch.2: Input ripple 100 mV/div.
Ch.3: Output ripple 20 mV/div.
Ch.4: Phase pin of TPS54680 (core) 5 V/div.
Ch.1: Phase pin of TPS54610 (I/O) 5 V/div.
Time: 1 µs/div

Figure 2-17. Input and Output Voltage Ripple and Main Switching Waveform at V_I = 5 V



Chapter 3

Board Layout

This chapter provides a description of the TPS54x80EVM-228 board layout and layer illustrations.

Topic **Page**

3.1 Board Layout 3-2

3.1 Layout

The board layout for the TPS54x80EVM-228 is shown in Figure 3-1 through Figure 3-4. The top side layer of the TPS54x80EVM-228 is laid out in a manner typical of a user application. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper.

The top layer contains the main power traces for V_I, V_O, and $V_{(phase)}$. Also on the top layer are connections for the remaining pins and a large area filled with ground. The noise sensitive parts R8, R19, C3, C7 near U1 and R6, R9, R20, C2, C6 near U2 have their own dedicated quiet ground areas which are separated from the high current paths. The second layer is dedicated ground plane. The third layer includes large areas for ground, V_I and V_O. The bottom layer filled by ground except some places occupied by signal traces. The top and bottom ground traces are connected to the internal ground planes with numerous vias placed around the board including 12 directly under the TPS54x80 and TPS54X10 devices to provide a thermal path from the PowerPAD™ land to ground.

The input ceramic capacitors (C4, C5, C8, and C9), bias decoupling capacitors (C6, C7), and boot strap capacitors (C10, C12) are all located as close to the ICs as possible. In addition, the compensation components are also kept close to the IC.

Figure 3-1. Top Side Assembly

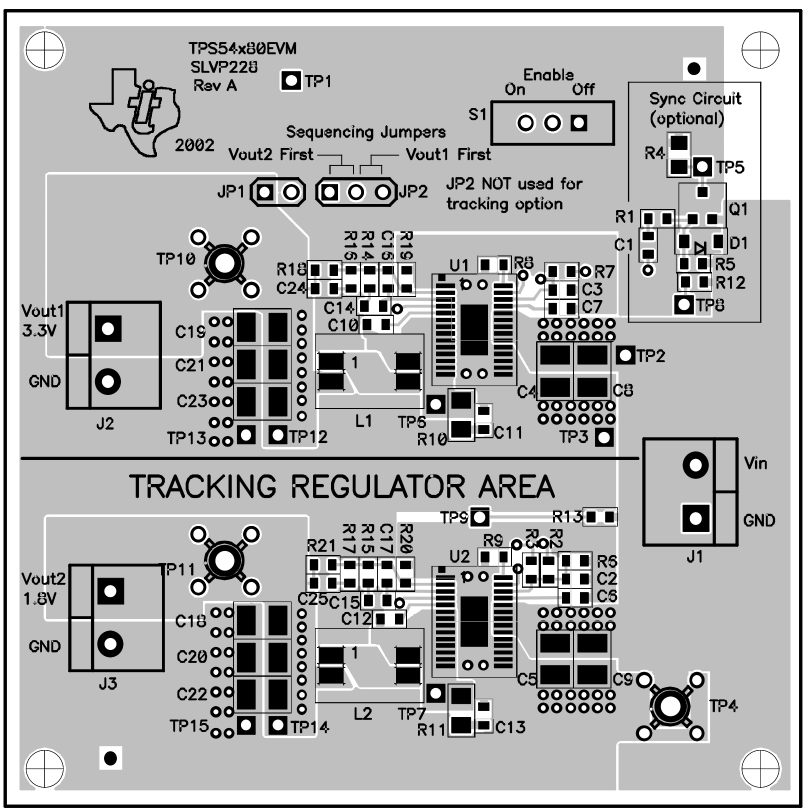


Figure 3-2. Top SIde Layout

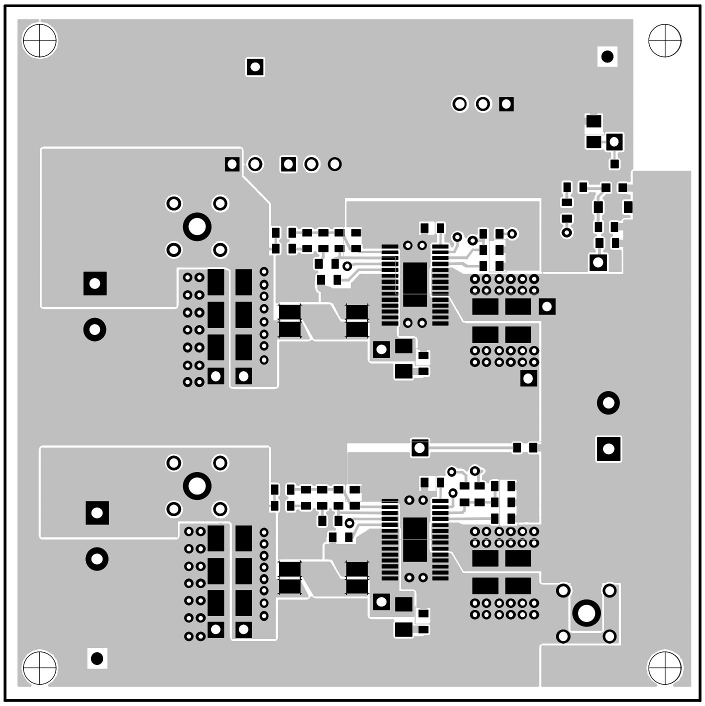


Figure 3-3. Internal Layer 2 Layout

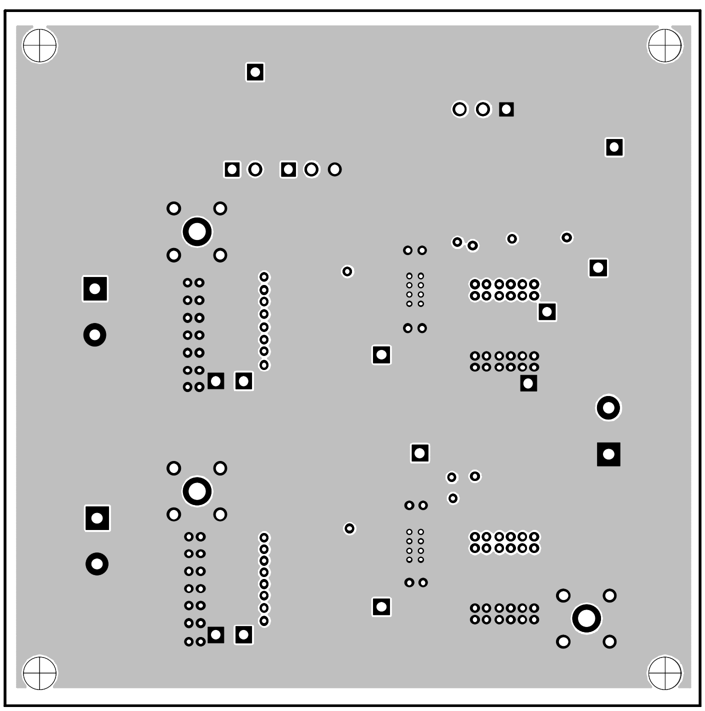


Figure 3-4. Internal Layer 3 Layout

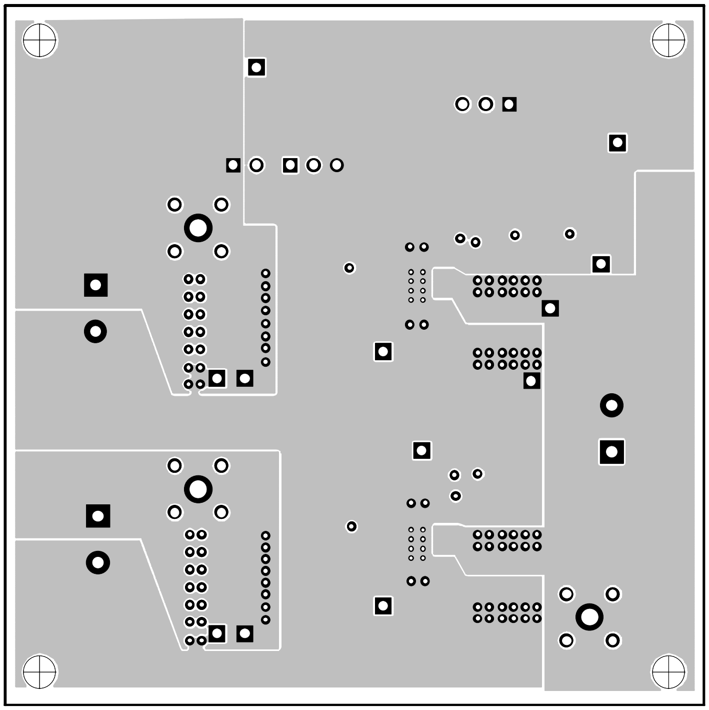
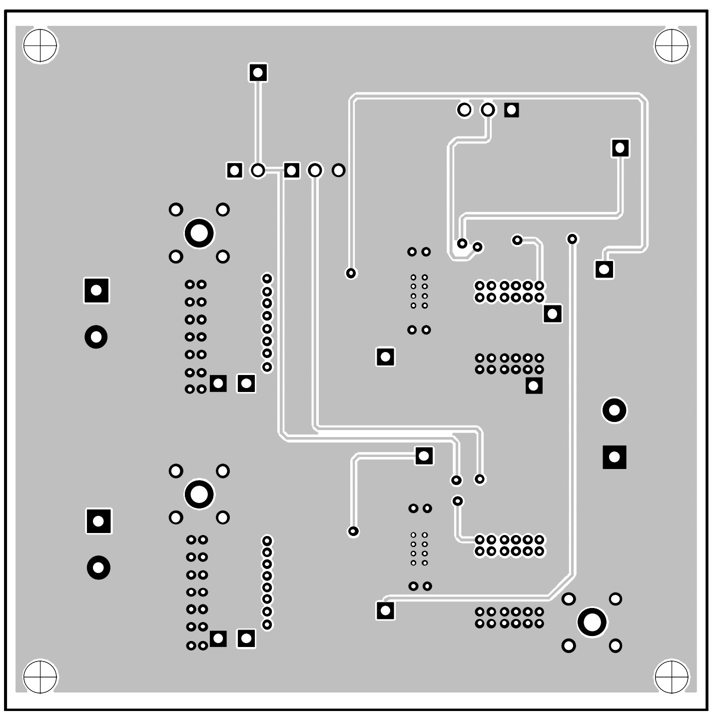


Figure 3-5. Bottom Side Layout (looking from top side)



Chapter 4

Schematic and Bill of Materials

The TPS54x80EVM-228 schematic and bill of materials are presented in this chapter.

Topic **Page**

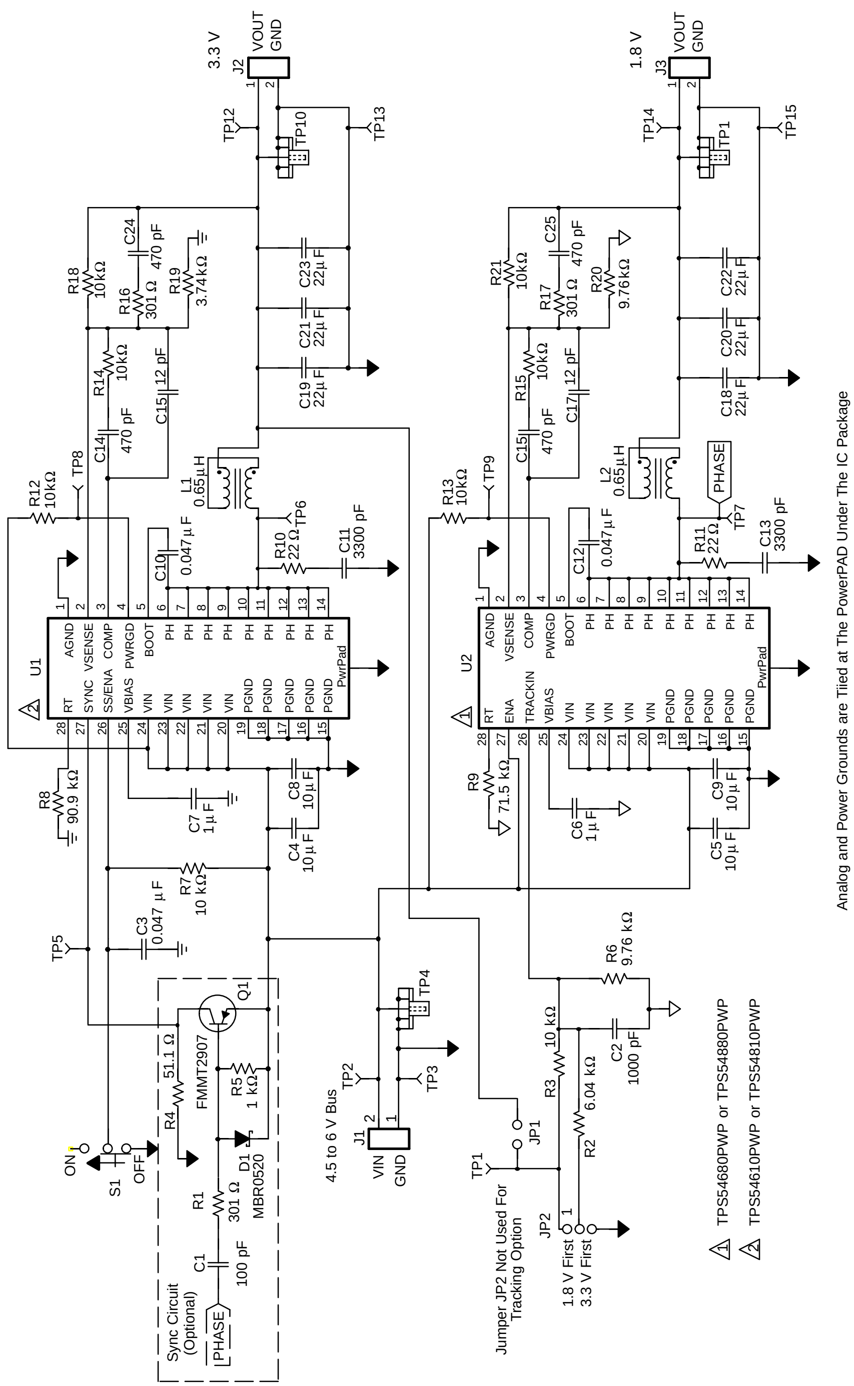
4.1 Schematic 4-2

4.2 Bill of Materials 4-3

4.1 Schematic

The schematic for the TPS54x80EVM-228 is shown in Figure 4-1.

Figure 4-1. TPS54x80EVM-228 Schematic



4.2 Bill of Materials

The bill of materials for the TPS54x80EVM-228 is given by Table 4-1.

Table 4-1. TPS54x80EVM-228 Bill of Materials

Count						
-1	-2	Ref Des	Description	SIze	MFR	Part Number
1	1	C1	Capacitor, ceramic, 100 pF, 50 V, C0G, 5%	603	Murata	GRM1885C1H101JA01
2	2	C11, C13	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H332K
4	4	C14, C15, C24, C25	Capacitor, ceramic, 470 pF, 50 V, X7R, 10%	603	Murata	GRM188R71H471KA01
2	2	C16, C17	Capacitor, ceramic, 12 pF, 50 V, NPO, 10%	603	Panasonic	EUC-V1H120KBV
6	6	C18, C19, C20, C21, C22, C23	Capacitor, ceramic, 22 µF, 6.3 V, X5R, 20%	1210	Taiyo Yu-den	JMK325BJ226MN
1	1	C2	Capacitor, ceramic, 1000 pF, 25 V, X7R, 10%	603	Murata	GRM188R71E102KA01
3	3	C3, C10, C12	Capacitor, ceramic, 0.047 µF, 25 V, X7R, 10%	603	Murata	GRM188R71E473KA01
4	4	C4, C5, C8, C9	Capacitor, ceramic, 10 µF, 16 V, X5R, 10%	1210	Taiyo Yu-den	LMK325BJ106KN
2	2	C6, C7	Capacitor, ceramic, 1.0 µF, 6.3 V, X5R, 10%	603	Murata	GRM188R60J105KA01
1	1	D1	Diode, Schottky, 500 mA, 20 V	SOD123	ON Semi	MBR0520LT1
3	3	J1, J2, J3	Terminal block, 2 pin, 15 A, 5, 1 mm	148830	OST	ED1609
1	1	JP1	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 × 2″	Sullins	PTC35SAAN
1	1	JP2	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 × 3″	Sullins	PTC36SAAn
2	2	L1, L2	Inductor, 0.65 µH, 12 A	0.340 × 0.250	Pulse	PA0277
1	1	Q1	Bipolar, PNP, 60 V, 600 mA, 0.25 W	SOT23	Zetex, Inc.	FMMT2907ATA
3	3	R1, R16, R17	Resistor, chip, 301 Ω, 1/16 W, 1%	603	Std	Std
2	2	R10, R11	Resistor, chip, 2.2 Ω, 1/4 W, 1%	1206	Panasonic	ERJ-8RQF2R2
1	1	R19	Resistor, chip, 3.74 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R2	Resistor, chip, 6.04 kΩ, 1/16 W, 1%	603	Std	Std
8	8	R3, R7, R12, R13, R14, R15, R18, R21	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R4	Resistor, chip, 51.1 Ω, 1/10 W, 1%	805	Std	Std
1	1	R5	Resistor, chip, 1.0 kΩ, 1/16 W, 1%	603	Std	Std
2	2	R6, R20	Resistor, chip, 9.76 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R8	Resistor, chip, 90.9 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R9	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	1	S1	Switch, 1P2T, slide, PC-mount, 200 mA	0.46 × 0.16	E_Switch	EG1218

Count						
-1	**-2**	**Ref Des**	**Description**	**SIze**	**MFR**	**Part Number**
9	9	TP1, TP2, TP5, TP6, TP7, TP8, TP9, TP12, TP14	Test point, red, 1 mm	0.038″	Farnell	240-345
3	3	TP3, TP13, TP15	Test point, black, 1 mm	0.038″	Farnell	240-333
3	3	TP4, TP10, TP11	Adaptor, 3,5 mm probe clip (or 131-5031-00)	72900	Tektronix	131-4244-00
1		U1	IC< IFET power controller, adj V, 6 A	PWP28	TI	TPS54610PWP
	1		IC, IFET power controller, adj V, 8 A	PWP28	TI	TPS54810PWP
1		U2	IC, tracking synchronous PWM switcher, 6 A	PWP28	TI	TPS54680PWP
	1		IC, tracking synchronous PWM switcher, 8 A	PWP28	TI	TPS54880PWP
1	1	—	PCB, 3 in × 3 in 0.62 in		Any	SLVP228
2	2	—	Shunt, 100 mil, black	0.100	3M	929950-00

Notes:
1) These assemblies are ESD sensitive, ESD precautions must be observed.
2) These assemblies must be clean and free from flux and all contaminant. Use of no clean flux is not acceptable.
3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4) Reference designators marked with an asterisk (**) cannot be substituted. All other componets can be substituted with equivalent MFG’s components.

Appendix A

Out of Phase Synchronization of I/O and Core SWIFT™ Family Regulators

This chapter provides additional information about the TPS54x80EVM-228.

If the core and I/O voltages are provided by the two dc/dc regulators running at a slightly different frequencies with the same input power supply, their input voltage ripple always includes a low frequency harmonic. Usually this effect is called the *beating* frequency. The input voltage ripple (Channel 2) of two nonsynchronized regulators running at frequencies about 15% apart is shown in Figure A-1.

Figure A-1. Input Voltage Ripple and Main Switching Waveforms at V_I = 5 V of Two Regulators Switching at 15% Apart Frequencies

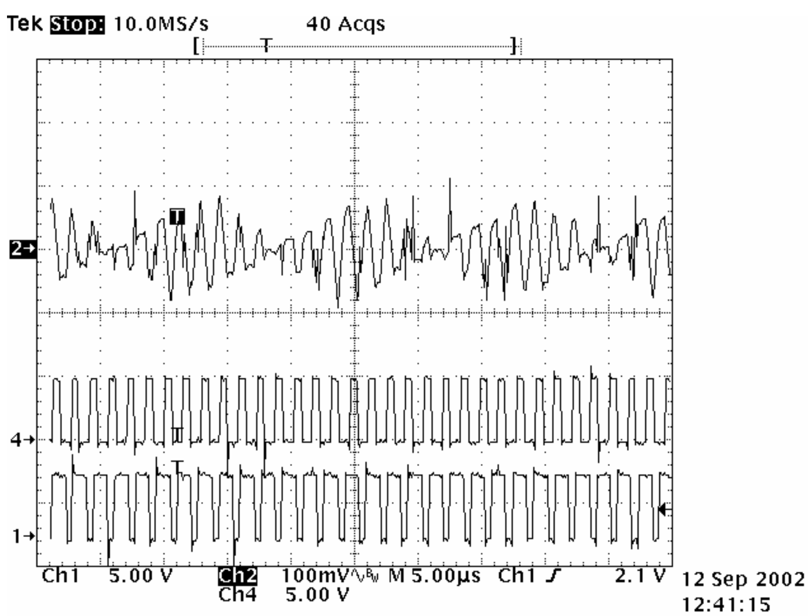
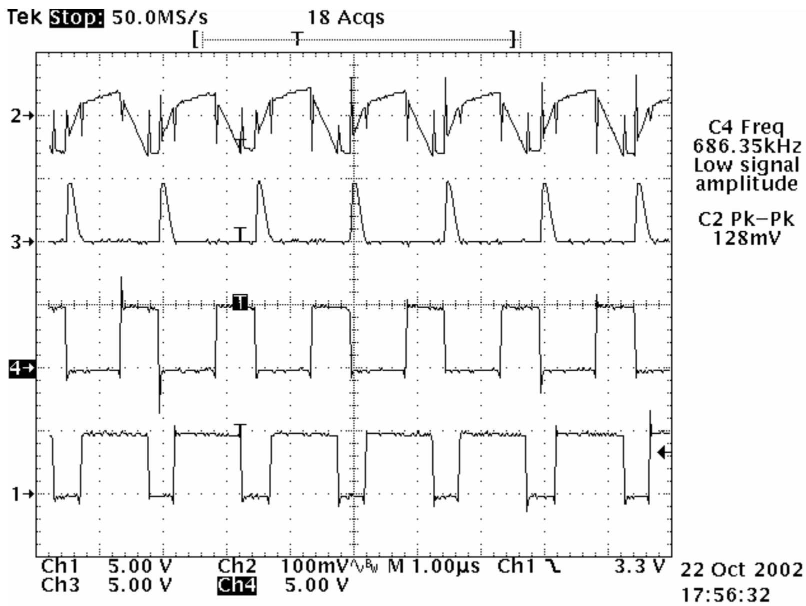


Figure A-2. Input Voltage Ripple (Ch.2),Sync Signal (Ch.3) and Switching Waveforms of Core Regulator (Ch.4) and I/O Regulator (Ch.1)



In many cases, this low frequency harmonic does not affect on overall performance of system. However, by synchronizing both switching regulators out of phase, it is possible to avoid the *beating* effect and to save some input capacitors because of ripple cancellation effect. This optional synchronization circuit is implemented into TPS54x80EVM-228. It includes the following parts shown separately in Figure 4-1: C1, R1, R4, R5, D1, Q1. This circuit takes the phase signal of core regulator U2 as its input, inverts this signal and synchronizes the I/O regulator U1 out of phase of regulator U2. The related waveforms are shown in Figure A-2.

The comparison of input voltage ripple for synchronized and nonsynchronized regulators is shown in Figure A-3 and Figure A-4 respectively

Figure A-3. Input Voltage Ripple (Ch.2)and Switching Waveforms of Synchronized Out of Phase Core Regulator (Ch.4) and I/O Regulator (Ch.1)

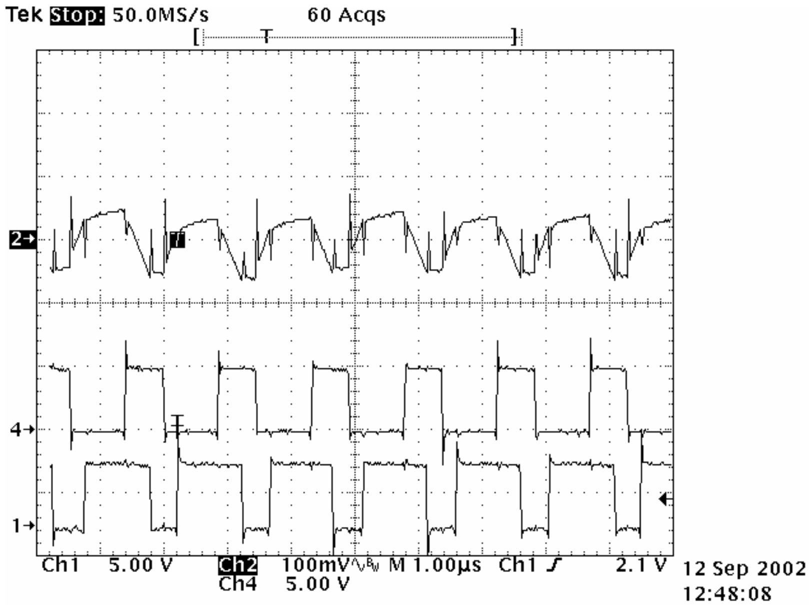
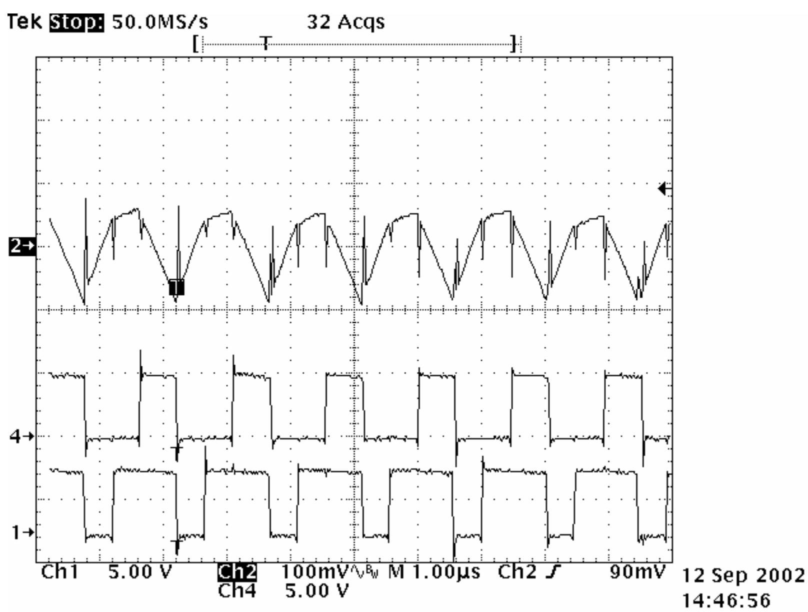


Figure A-4. Input Voltage Ripple (Ch.2 and Switching Waveforms of Nonsynchronized Core Regulator (Ch.4) and I/O Regulator (Ch.1)



It can be seen that the input voltage ripple of synchronized regulators is 100 mV peak-to-peak, while the input voltage ripple of nonsynchronized regulators is 150 mV peak-to-peak. The ripple cancellation effect is the most significant when both regulators have roughly the same output current and the duty cycles complement each other.